AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A delay analysis system for making a delay analysis of a logic circuit, said system ~~having~~ comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits; and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library,

wherein, for at least one circuit of said plurality of circuits, said library further comprises logical operation information, wherein delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein said delay time information for each signal path of the logical circuit of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to logical operation information,

wherein the delay analyzing module analyzes the delay of the logical circuit based on the delay time information in said delay analysis library.

2. (currently amended): A delay analysis system for making a delay analysis of a logic circuit, said system ~~having~~ comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits; and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library,

wherein, for each of said plurality of circuits, said library further comprises logical operation information, wherein delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of said plurality of circuits, and wherein said delay time information for each signal path of said plurality of circuits is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to logical operation information for said plurality of circuits,

wherein the delay analyzing module analyzes the delay of the logical circuit based on the delay time information in said delay analysis library.

3. (currently amended): A method for making a delay analysis of a logic circuit, comprising:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation ~~delay~~ information, wherein delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits, said delay time information for each signal path of said at least one

circuit is based upon logical state transitions at said input terminals and corresponding logical

state transitions at each output terminal as represented by logical operation information for said

at least one circuit; and

if the logic circuit comprises said at least one circuit, selecting ~~the~~ a delay time of each

path of said at least one circuit from said delay time information, wherein if a selected output

terminal transitions from a low state to a high state, said delay time is selected based on the input

terminal whose logical transition triggers said low state to high state transition of said selected

output terminal according to the logical operation information, or if a selected output terminal

transitions from a high state to a low state, said delay time is selected based on the input terminal

whose logical transition triggers said high state to low state transition of said selected output

terminal according to the logical operation information.

4. (currently amended): A computer-readable medium having stored thereon a program

comprising computer instructions that, when executed on a computer, perform a process for

executing a delay analysis method for a logic circuit, said computer-readable medium causing a

computer to execute said method, wherein said method comprises:

referencing a delay analysis library for a plurality of circuits, said delay analysis library

comprising connection information, delay time information and logic operation ~~delay~~

information, wherein delay time information is provided for a signal path from input terminals of

a logical circuit and wherein ~~a~~ delay time information is specific to an input terminal logical state

transition and resulting logical state transition at each output terminal for at least one circuit of

said plurality of circuits, said delay time information for each signal path of said at least one

circuit is based upon logical state transitions at said input terminals and corresponding logical

state transitions at each output terminal as represented by logical operation information for said at least one circuit;

if said logic circuit comprises said at least one circuit, selecting ~~the~~ a delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the input terminal whose logical transition triggers said low state to high state transition of said selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the input terminal whose logical transition triggers said high state to low state transition of said selected output terminal according to the logical operation information; and

performing a delay calculation to determine a propagation delay time using said selected delay time of said at least one circuit.

5. (new): The delay analysis system as set forth in claim 1, wherein the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed.

6. (new): The delay analysis system as set forth in claim 5, wherein the logical circuit is an AND gate, and when the logical operation information of the AND gate in the delay analysis library indicates that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals, and at a time at which the second clock signal among

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the two clock signals is input, the state is LOW which is regarded to be the same state as the first signal state, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determines that no further delay analysis needs to be performed in this case.